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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/722,752 | 11/26/2003 | Toshinobu Nakao | 967_038 | 7293 |

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| EXAMINER | |
|---|---|
| TRIMMINGS, JOHN P | |
| **ART UNIT** | **PAPER NUMBER** |
| 2138 | |

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/722,752 | NAKAO ET AL. | |
| | Examiner | Art Unit | |
| | John P. Trimmings | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-15* is/are allowed.

6)☒ Claim(s) *1-8 and 11* is/are rejected.

7)☒ Claim(s) *1,4,9,10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-15 are presented for examination.

### *Priority*

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 3/12/2003. It is noted, however, that applicant has not filed a certified copy of the English translation of the application as required by 35 U.S.C. 119(b).

### *Information Disclosure Statement*

2. The examiner acknowledges the applicant's Information Disclosure Statement and has considered said disclosure.

### *Specification*

3. The disclosure is objected to because of the following informalities:

Page 31 paragraph [0118], line 1 should be corrected to read, "... scan storage element ~~67~~ 27 performs ...".

Page 31 paragraph [0118], line 5 hould be corrected to read, "... the normal data ~~11~~ 711 to the ...".

Appropriate correction is required.

### *Drawings*

4. The drawings are objected to because FIG.8 box 800 contains a typographical error. The last line within box 800 should be corrected to read, "... of a n pieces of scan ...".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Objections***

5. Claims 1 and 4 are objected to because of the following informalities: The claims contain limitations that are in parentheses. Any matter within parenthesis is not given patentable weight, and so the examiner requests that the applicant remove the

parentheses and reword the contents in order to properly apply the limitations to the claim. Appropriate correction is required.

6. Claim 1 is objected to under 37 CFR 1.75 (Claims), paragraph (i); "Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation". Appropriate correction is required.

7. Claim 10 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim ("Claims in dependent form shall be construed to include all the limitations of the claim incorporated by reference into the dependent claim"). The subject claim is objected to because it is worded so as to remove the limitations of the prior claims. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant has worded the claim to functionally encompass the circuit of an admitted prior art (see FIG.18 and FIG.20), and so the examiner is not

sure of what it is that the applicant wishes to patent, because the applicant is barred from patenting the prior art (see page 29, paragraph 111; "Since the scan test circuit according to the third embodiment (Claim 10) is constructed as described above, the circuit construction becomes the same as that of the conventional scan test circuit shown in FIG. 18.").

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnston et al. (herein Johnston), U.S. Patent No. 6877123.

As per Claim 1:

Johnston teaches a scan test control method for a scan test circuit having a scan chain including n pieces of scan storage elements (column 5 lines 22-24), wherein a frequency of a first clock to be used for shifting data into the first to n-1th scan storage elements (see FIG.3 CLOCK OUTPUT WITHIN SAME DOMAIN). Note that the diagram shows 2 "SHIFT" clocks, and the 3rd shift being the "LAUNCH" clock while maintaining

"SCAN ENABLE" (see column 5 lines 39-42 and column 10 lines 17-24 for "SCAN LAUNCH"). And further, a frequency of a second clock to be used for shifting data into the n-th scan storage element and performing normal operation (FIG.3 LAUNCH, CAPTURE), are independently controlled (column 6 lines 27-49, column 7 lines 50-52 and see FIG.1).

As per Claim 2:

Johnston further teaches the scan test control method of claim 1, wherein the frequency of the first clock and the frequency of the second clock are different from each other (column 6 lines 27-49).

As per Claim 3:

Johnston further teaches the scan test control method of claim 1, wherein the frequency of the second clock is a clock frequency to be used in the normal operation (column 6 lines 27-49).

As per Claim 4:

Johnston teaches a scan test circuit comprising: a scan chain having n pieces of scan storage elements (column 5 lines 22-24); a scan clock generation circuit (see FIG.1 116, 128, 130, 132, 134) for receiving first (FIG.1 110) and second clocks (FIG.1 112), and outputting one of the first clock and the second clock as a scan clock (FIG.1 134) for operating the plural scan storage elements (TARGET CIRCUIT); and a selection circuit for selecting the first clock as the scan clock to be used for shifting data into the first to n-1th scan storage elements (see FIG.3 CLOCK OUTPUT WITHIN SAME DOMAIN and column 10 lines 17-24), and selecting the second clock as the

scan clock to be used for shifting data into the n-th scan storage element and performing normal operation (column 10 lines 25-35).

As per Claim 5:

Johnston further teaches the scan test circuit of claim 4 further including a scan selection signal generation circuit (FIG.2) which receives, from the outside, a scan selection external signal (SCAN ENABLE CONTROL PIN) for switching between normal operation and scan test operation (column 10 lines 17-24), and generates a scan selection internal signal (SCAN ENABLE) for selectively switching between normal operation and operation for shifting data into the plural scan storage elements (column 10 lines 17-45) in synchronization with the second clock (VCO Clock controls FIG.1 112 and 210).

As per Claim 6:

Johnston further teaches the scan test circuit of claim 5, wherein the scan selection signal generation circuit generates a control signal for generating an arbitrary number of the second clocks (see column 13 lines 40-59).

As per Claim 7:

Johnston further teaches the scan test circuit of claim 6, wherein the scan selection signal generation circuit switches between a first timing at which the scan clock generation circuit generates the second clock as the scan clock (VCO Clock controls FIG.1), and a second timing at which the scan selection internal signal is generated (FIG.1 210 controls the scan enable internal signal, see column 10 lines 17-45).

As per Claim 8:

Johnston further teaches the scan test circuit of claim 7, wherein the scan selection signal generation circuit arbitrarily selects one of the first timing and the second timing (see column 10 lines 17-45).

As per Claim 11:

Johnston teaches a scan test control method for a scan test circuit comprising a first block having a first scan test circuit that operates in synchronization with first and second clocks, and a second block having a second scan test circuit that is synchronized with only the first clock, wherein the normal operation time of the scan test in the first block is different from the normal operation time of the scan test in the second block (column 7 lines 53-67 and column 8 lines 1-13).

10. Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Ahanin et al. (herein Ahanin), U.S. Patent No. 5285153. Ahanin teaches the scan test circuit of claim 9, wherein when generating a scan test pattern, the scan clock generation circuit is replaced with a circuit (FIG.2 108, 110) that connects a terminal to which the first clock is input (FIG.2 12j), directly to a signal line from which the scan clock is output (FIG.2 120 "CLOCK"), the scan selection signal generation circuit is replaced with a circuit (a wire) that connects a terminal to which the scan selection external signal is input (FIG.2 12d), directly to a signal line from which the scan selection internal signal is output (FIG.2 120 "SELECT"), and the storage element is replaced with a circuit (a wire) that connects a signal line to which data in the storage element is input (FIG.2 12e), directly

to a signal line from which the data is output (FIG.2 "DB"). In view of the rejection of this claim under 35 USC 112 second paragraph, and the objection to this claim (see above) the examiner rejects the claim under the reference art because the claim has been reduced by limitation to the circuit in FIG.2.

***Allowable Subject Matter***

11. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 12-15 are allowed. The following is an examiner's statement of reasons for allowance: The referenced art of Johnston and Ahanin teach a 1st block operating under a 1st and 2nd clock and a 2nd block that operates under a 1st clock, comprising 1st storage elements synchronous with the 1st clock, 2nd storage elements synchronous with the 1st and 2nd clocks, but fail to teach, suggest or disclose a selector provided between the two blocks that controls the path of data between the two blocks.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

jpt

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